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10/710,725	07/30/2004	Hui-Hua Kuo	MTKP0084USA	4724

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EXAMINER
HOLDER, ANNER N

ART UNIT	PAPER NUMBER
2621	

NOTIFICATION DATE	DELIVERY MODE
02/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,725	KUO ET AL.	
	Examiner	Art Unit	
	Anner Holder	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (Kim) US 7,088,772 B2.

3. As to claim 1, Kim teaches the steps of: (a) storing a plurality of first vertical predictors of a first block into a storing column of a first memory device, and storing a plurality of first horizontal predictors of a second block into a storing row of the first memory device; [Abstract; Fig. 5; Col. 4 Lines 33-43; Col. 7 Lines 48-67] (b) performing a prediction operation for generating a plurality of target vertical predictors and a plurality of target vertical predictors of a first target block according to the first vertical predictors and the first horizontal predictors, wherein the first target block is adjacent to the first and second blocks, and the first block and the first target block are located at the same row; [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57] and (c) updating the storing column of the first memory device by the target vertical predictors, and updating the storing row of the first memory device by the target horizontal predictors. [Col. 8 Lines 3-20; Col. 4 Lines 48-61; storing memory in the upper right memory strongly suggest vertical predictors storage; storing in the lower right and lower left strongly suggest horizontal predictors storage]

4. As to claim 2, Kim teaches the first and second blocks and the first target block are located within different macro-blocks each comprising a plurality of blocks, the first target block is not located at a bottom row of a corresponding macro-block, [Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) updates the storing column by the target vertical predictors and updates the storing rows by the target horizontal predictors. [Abstract; Fig. 5; Col. 7 Lines 48-67]

5. As to claim 3, Kim teaches step (a) further comprises storing a diagonal predictor for the first target block into a memory cell of the first memory device, [Abstract; Col. 4 Lines 33-43] step (b) generates the target horizontal predictors and the target vertical predictors according to the diagonal predictor, the first vertical predictors, and the first horizontal predictors, [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) further comprises updating the memory cell of the first memory device by a diagonal predictor for a second target block being processed after the first target block, wherein the first and second target blocks are located within the same macro-block. [Abstract; Fig. 5; Col. 7 Lines 48-67]

6. As to claim 4, Kim teaches the first block and the first target block are located within a macro-block comprising a plurality of blocks, the second block is located within another macro-block comprising a plurality of blocks, the first target block is not located at a bottom row of the corresponding macro-block, the first vertical predictors are stored in a first part of the storing column, the first horizontal predictors are stored in a first part of the storing row, [Abstract; Col. 4 Lines 33-43; Fig. 5; Fig. 6; Col. 7 Lines 50-67] and step (c) updates the first part of the storing

column by the target vertical predictors and updates a second part of the storing row by the target horizontal predictors. [Abstract; Fig. 5; Col. 7 Lines 48-67]

7. As to claim 5, Kim teaches step (a) further comprises storing a diagonal predictor for the first target block into a memory cell of the first memory device, [Abstract; Col. 4 Lines 33-43] step (b) generates the target horizontal predictors and the target vertical predictors according to the diagonal predictor, the first vertical predictors, and the first horizontal predictors, [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) further comprises updating the memory cell of the first memory device by a diagonal predictor for a second target block being processed after the first target block, wherein the first and second target blocks are located within the same macro-block. [Abstract; Fig. 5; Col. 7 Lines 48-67]

8. As to claim 6, Kim teaches the first block is located within a macro-block comprising a plurality of blocks, the second block and the first target block are located within another macro-block comprising a plurality of blocks, the target block is located at a bottom row of the corresponding macro-block, [Abstract; Col. 4 Lines 33-43; Fig. 5; Fig. 6; Col. 7 Lines 50-67] and step (c) updates the storing column by the target vertical predictors without updating the storing row. [Abstract; Fig. 5; Col. 7 Lines 48-67]

9. As to claim 7, Kim teaches (a) further comprises storing a diagonal predictor for the first target block into a memory cell of the first memory device, [Abstract; Col. 4 Lines 33-43] step (b) generates the target horizontal predictors and the target vertical predictors according to the diagonal predictor, the first vertical predictors, and the first horizontal predictors, [Abstract; Fig.

6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) further comprises updating the memory cell of the first memory device by a diagonal predictor for a second target block being processed after the first target block, wherein the first and second target blocks are located within the same macro-block. [Abstract; Fig. 5; Col. 7 Lines 48-67]

10. As to claim 8, Kim teaches storing the target horizontal predictors into a second memory device. [Abstract; Col. 4 Lines 33-43]

11. As to claim 9, Kim teaches the first and second blocks and the first target block are located within a macro-block comprising a plurality of blocks, the first target block is located at a bottom row of the macro-block, [Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) updates the storing column by the target vertical predictors without updating the storing row. [Abstract; Fig. 5; Col. 7 Lines 48-67]

12. As to claim 10, The predictive decoding method of claim 9 wherein step (a) further comprises storing a diagonal predictor for the first target block into a memory cell of the first memory device, [Abstract; Col. 4 Lines 33-43] step (b) generates the target horizontal predictors and the target vertical predictors according to the diagonal predictor, the first vertical predictors, and the first horizontal predictors, [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and step (c) further comprises updating the memory cell of the first memory device by a diagonal predictor for a second target block being processed after the first target block, wherein the first and second target blocks are not located within the same macro-block. [Abstract; Fig. 5; Col. 7 Lines 48-67]

13. As to claim 11, Kim teaches storing the target horizontal predictors into a second memory device. [Abstract; Col. 4 Lines 33-43]

14. As to claim 12, Kim teaches the picture conforms to an MPEG specification. [Col. 1 Lines 29-49; Col. 6 Lines 50-57]

15. As to claim 13, Kim teaches the vertical and horizontal predictors of a block lie in the most left column and top row of the block, and the horizontal predictors and the vertical predictors of the block respectively comprise a DC coefficient and a plurality of AC coefficients. [Fig. 6; Col. 8 Lines 21-28 – predictors can be classified as DC and AC coefficients depending upon the spatial configuration]

16. As to claim 14, (a) generating a plurality of predictors of the first block according to a first adjacent block and a second adjacent block; [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] (b) after proceeding with step(a), storing the predictors of the first block into the first memory device; [Abstract; Col. 4 Lines 33-43] (c) after proceeding with step(b), generating a plurality of predictors of the second block according to a third adjacent block and the first block; [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 – 57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] (d) after proceeding with step(c), storing the predictors of the second block into the first memory device; [Abstract; Col. 4 Lines 33-43] (e) after proceeding with step(d), generating a plurality of predictors of the third block according to a fourth adjacent block and the first block; [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] (f) after proceeding with step(e), storing the predictors of the third block into the first memory device and the second

memory device; [Abstract; Col. 4 Lines 33-43] (g) after proceeding with step (f), generating a plurality of predictors of the fourth block according to the second block and the third block; [Abstract; Fig. 6; Fig. 7; Col. 6 Lines 50 –57; Figs. 3-4d; Figs. 6-7; Col. 4 Lines 50-55; Col. 8 Lines 21-45] and (h) after proceeding with step(g), storing the predictors of the fourth block into the first memory device and the second memory device [Abstract; Col. 4 Lines 33-43; wherein Col. 4 Lines 48-61; storing memory in the upper right memory strongly suggest vertical predictors storage; storing in the lower right and lower left strongly suggest horizontal predictors storage)

17. As to claim 15, The method of claim 14 wherein a plurality of predictors for each block comprise a plurality of vertical predictors, a plurality of horizontal predictors, and a diagonal predictor, and the method further comprises: (i) in step(b), storing a plurality of vertical predictors of the first block into a storing column of the first memory device, and storing a plurality of horizontal predictors of the first block into a storing row of the first memory device; [Abstract; Col. 4 Lines 33-43] (j) in step(d), storing a plurality of vertical predictors of the second block into the storing column of the first memory device, and storing a plurality of horizontal predictors of the second block into the storing row of the first memory device; [Abstract; Col. 4 Lines 33-43] (k) in step (f), storing a plurality of vertical predictors of the third block into the storing column of the first memory device, and storing a plurality of horizontal predictors of the third block into the second memory device; [Abstract; Col. 4 Lines 33-43] and (l) in step (h), storing a plurality of vertical predictors of the fourth block into the storing column of the first memory device, and storing a plurality of horizontal predictors of the fourth block into the second memory device. [Abstract; Col. 4 Lines 33-43]

18. As to claim 16, Kim teaches step (j), the vertical predictors of the second block stored into the storing column of the first memory device replace the vertical predictors of the first block initially stored in the storing column, [Abstract; Col. 4 Lines 33-43] and in step (l), the vertical predictors of the fourth block stored into the storing column of the first memory device replace the vertical predictors of the third block initially stored in the storing column. [Abstract; Col. 4 Lines 33-43]

19. As to claim 17, Kim teaches5 wherein the vertical and horizontal predictors of a block lie in the most left column and top row of the block, and the vertical predictors and the horizontal predictors of the block respectively comprise a plurality of AC coefficients and a DC coefficient. [Fig. 6; Col. 8 Lines 21-28 – predictors can be classified as DC and AC coefficients depending upon the spatial configuration]

20. As to claim 18, Kim teaches the first block is at an upper-left site of the macro-block, the second block is at an upper-right site the macro-block, the third block is at a lower-left site of the macro-block, and the fourth block is at a lower-right site of the macro-block. [Figs. 3-7; Col. 4 Lines 48-55; Col. 7 Lines 12-27, 48-67]

21. As to claim 19, Kim teaches the first adjacent block is at a left side of the first block, the second adjacent block is at an upper side of the first block, the third adjacent block is at an upper side of the second block, and the fourth adjacent block is at a left side of the third block. [Abstract; Figs. 3-7; Col. 4 Lines 50-55; Col. 7 Lines 37-67]

22. As to claim 20, Kim teaches the macro-block conforms to an MPEG specification. [Col. 1 Lines 29-49]

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anner Holder whose telephone number is 571-270-1549. The examiner can normally be reached on M-Th, M-F 8 am - 3 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANH 02/15/08

TUNG VO
PRIMARY EXAMINER